Area-Efficient Hardware Design of a Tunable Digital Filter for Ultra-High Density Neural Recording Systems
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Abstract
As microelectrode arrays (MEAs) with rapidly increasing channel densities are developed to investigate increasingly large ensembles of neurons, the challenges of processing the data in real time has scaled accordingly. For our target 256x256 channel recording system, the data rate of approximately 3 GB/s renders processing schemes considered efficient in conventional applications entirely infeasible for this device. Here, we propose a highly efficient and modular infinite-impulse response (IIR) filter design implemented on field-programmable gate arrays (FPGAs) with stringent chip area and processing latency constraints. Strategic optimization of tradeoffs in area, timing, and precision allow for the implementation, in inexpensive FPGAs, of a pipelined band-pass IIR filter with tunable cutoff frequencies for all channels on the device.

Keywords
IIR filter, microelectrode array, extracellular recording, high density, real-time